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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/710,272
Filing Date: June 30, 2004
Appellant(s): DORIS ET AL.

Frederick E. Cooperrider

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed April 26, 2010 appealing from the Final Office action mailed Dec. 14, 2009.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

Claims 1-4, 6, 10-15 and 23-30.

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

2004/0173812	Currie et al.	9-2004
2005/0242395	Chen et al.	11-2005
2004/0108559	Sugii et al.	6-2004

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-4, 6, 10-15, 23-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Currie et al. 2004/0173812, in view of Sugii et al. 2004/0108559, or Chen et al. 2005/0242395, previously cited.

The reference discloses:

Currie et al. teaches a method of forming an electronic device, said device comprising a FinFET (Fin Field Effect Transistor) containing a plurality of fins interconnected by fin connectors (see para. 87), said method comprising:

forming at least one localized stressor region (recess) 144, 148 within said device (see figs. 10D-10E, para. 16, 77), said at least one localized stressor region 150 being located on one of said fin connectors 144, 148 (at the end of fin 18) as a region of stressor material 150 filling in an interior portion of said fin connector 144, 148 (at the end of fin 18, para. 77, 87 teach that embodiments of this invention may also be

applicable to transistors with multiple or wrap-around gates. Examples of these include fin-FETs, tri-gate FETs, omega-FETs, and double-gate FETs (the channels of which may be oriented horizontally or vertically), hence, the localized stressor trench region 150 (SiGe, see figure 10E) located on the fin connector (at the end of fin 18) between transistor 106 and transistor 106' can be applicable to the FinFET (Fin Field Effect Transistor). A plurality of fins 18 interconnected by fin connectors, such as fin-FETs, tri-gate FETs etc., Currie teaches: fin includes channel 108 and fin 18, fin connector/pad (source/drain) 150, gate 110, gate dielectric 114. see Chen et al. teaches in figs. 3-5, fin-FET having fin connectors 36 or S or D connecting fin 12 or 21, Sugii et al. teaches in figure 28, fin-FET having fin connectors 4 connecting fin 5.

Regarding claim 2. The method of claim 1, wherein said at least one localized stressor region 144/150 comprises a first localized stressor region 144/150, said method further comprising:

forming a second localized stressor region 148/150 within said device, said first localized stressor region and said second localized stressor region causing a region (channel) 108 there between to be stressed, para. 77, fig. 10E.

Regarding claim 3. The method of claim 2, wherein said first localized stressor region and said second localized stressor region comprise a same type material, para. 77.

Regarding claim 4. The method of claim 3, wherein said same type material comprises one of a compressive stressor material and a tensile stressor material, para. 77.

Regarding claim 6. The method of claim 2, wherein said first and second localized stressor regions are formed on said fin connectors of said FinFET as regions of stressor material filling in interior portions of respective two fin connectors, para. 77, 87.

Regarding claim 10. The method of claim 4, wherein said same type material comprises a compressive material and primary charge carriers in said region being stressed comprise holes, para. 77, 68.

Regarding claim 11. The method of claim 4, wherein said same type material comprises a tensile material and primary charge carriers in said region being stressed comprise electrons, para. 77, 68.

Regarding claim 12. The method of claim 2, wherein said region being stressed causes a carrier mobility in said stressed region to be one of increased and decreased, relative to a carrier mobility in a region without said stress, para. 6, 35.

Regarding claim 13. The method of claim 1, wherein said device comprises one of a plurality of devices in an electronic circuit, said method further comprising: selectively providing a blocking mask 32 over devices in said electronic circuit which are not to receive said at least one localized stressor region, fig. 2.

Regarding claim 14. A method of forming a stress region in an electronic device, said device comprising a FinFET (Fin Field Effect Transistor) containing a plurality of fins interconnected by fin connectors (see para. 87 and see figs. 3-5 of Chen), said method comprising:

forming a first localized stressor region 144/150 (at the end of fin 18, see figs. 10D-10E, para. 77, 87) within said device on a first fin connector (at the end of fin 18) as comprising a first region of stressor material filling 150 in an interior portion of said first fin connector (at the end of fin 18); and forming a second localized stressor region 148/150 within said device on a second fin connector (at the end of fin 18) as comprising a second region of stressor material 150 filling in an interior portion of said second fin connector, said first localized stressor region and said second localized stressor region causing a region 108 there between to be stressed, para. 77, 87 teach that embodiments of this invention may also be applicable to transistors with multiple or wrap-around gates. Examples of these include fin-FETs, tri-gate FETs, omega-FETs, and double-gate FETs (the channels of which may be oriented horizontally or vertically), hence, the localized stressor trench region 144/150, 148/150 (see figures 10D-10E) located on the fin connector (at the end of fin 18) between transistor 106 and transistor 106' that can be applicable to the FinFET (Fin Field Effect Transistor). A plurality of fins 18 interconnected by fin connectors, such as fin-FETs, tri-gate FETs etc. Currie teaches: fin includes channel 108 and fin 18, fin connector/pad (source/drain) 150, gate 110, gate dielectric 114. see Chen et al. teaches in figs. 3-5, fin-FET having fin connectors 36 or S or D connecting fin 12 or 21, Sugii et al. teaches in figure 28, fin-FET having fin connectors 4 connecting fin 5.

Regarding claim 15. The method of claim 14, wherein said region being stressed causes a carrier mobility in said stressed region to be one of increased and decreased, relative to a carrier mobility in a region without said stress, para. 6, 35, 68.

Regarding claim 23. The method of claim 1, wherein at least one of said at least one localized stressor region 150 interacts with a stressed region 55a or 55b located outside said device, fig. 10E.

Regarding claim 24. The method of claim 1, wherein said at least one localized stressor region is used to generate one of a compression stress and a tensile stress, para. 77.

Regarding claim 25. The method of claim 1, wherein said at least one localized stressor region 150 is located within said device to generate a stress that enhances a performance of said device, para. 16, 77.

Regarding claim 26. The method of claim 25, wherein said performance enhancement comprises an increase in a carrier mobility, para. 6, 35, 77.

Regarding claim 27. The method of claim 25, wherein said performance enhancement comprises a decrease in a carrier mobility, para. 6, 35, 77.

Regarding claim 28. The method of claim 1, wherein said at least one localized stressor region is located to generate a stressed region in at least one of a direction parallel to a current flow and perpendicular to a current flow, para. 77, figs. 10E.

Regarding claim 29. The method of claim 1, wherein said at least one localized stressor region 150 is used to create a symmetrically stressed region, fig. 10E, para. 77.

Regarding claim 30. The method of claim 1, wherein said at least one localized stressor region is used to create an asymmetrically stressed region, para.77.

The difference between the reference(s) and the claims are as follows: Currie et al. teaches forming localized stressor trench regions on the fin connectors between

transistors but does not show fin-FET having fin connectors in the drawing. However, Sugii et al. teaches in figure 28, fin-FET having fin connectors. Sugii et al. also teaches at figs. 13-14, 19-29, para. 123-153, the source/drain regions 4 is a part of fin connector and forming localized stressor 5 on the of the fin connector 4. Sugii et al. also teaches forming a localized stressor 5 on the channel region, See figs. 13-14, 19-29. Chen et al. teaches at figs. 3-5 and para 26, a fin-FET having fin connectors and forming silicide layer on the fin connector.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have recognized that localized stressor trench (recess) region can be formed on a fin connector as shown in fig. 28 of Sugii et al. or figs. 3-5 of Chen et al. because fin connector connects source/drain regions of two FET transistors together.

(10) Response to Argument

Issue #1:

THE REJECTION FOR INDEPENDENT CLAIM 1, AS BASED ON CURRIE, FURTHER IN VIEW OF EITHER SUGII OR CHEN

Appellants contend that in summary, Appellants respectfully submit that the prior art rejection of record fails to demonstrate all elements of the claimed invention, since there is no demonstration of providing a localized stressor on the fin connectors of a finFET as a filled-in region on the interior portion of the finFET fin connectors.

This is not found persuasive because Currie clearly teaches in figures 10A-10E, para. 77, forming at least one localized stressor region 150 within (inside trench/recess) said device (see fig. 10E), the at least one localized stressor region 150 being located on one of fin connectors ((**at the end of fin 18,** note: 55a, 55b, 55c, 55d are isolation structures outside transistor), thus 150 is a part of fin connector, see para. 87:fin-FET, and see figure 5 of Chen: fin 21, fin connectors S(source)/D(drain), or figures. 27A-27C, 28 of Sugii: fin 5, fin connector 4 plus end portion of 5)) as a region of stressor material 150 filling in an interior portion of said fin connector (**at the end of fin 18**).

Currie teaches at **para. 87**, that embodiments of this invention may also be applicable to transistors with multiple or wrap-around gates. Examples of these include **fin-FETs**, tri-gate FETs, omega-FETs, and double-gate FETs (the channels of which may be oriented horizontally or vertically), hence, the localized stressor trench region 150 (see fig. 10E) located on the fin connector (at the end of fin 18, note: layer 55a, 55b are an isolation region outside the transistor) that is applicable to the FinFET (Fin Field Effect Transistor). A plurality of fins 18 interconnected by fin connectors, such as fin-FETs, tri-gate FETs etc. Currie et al. teaches, fin includes channel 108 and fin 18, fin connector/pad (source/drain at the end of fin 18) 150, gate 110, gate dielectric 114.

Chen et al. teaches in figure 5, S (source) and D (drain) of fin-FET are part of fin connectors connecting with fin 21.

Sugii et al. teaches in figure 27A-27C, 28, fin-FET having source/drain fin/fin connector 5/4/12.

Thus, it would have been obvious to one having ordinary skill in the art at the time of invention was made to have recognized Currie's localized recess regions 144, 148 (within the device, fig. 10D) filled with strain/stress material 150 formed at the end of fin 18 (fig. 10B) of source/drain regions 102/104 would be obvious as a part of fin connector as taught by Chen et al. in figure 5 of Chen, or by Sugii et al. in figures 27A-27C and 28 of Sugii because source and drain regions are part of fin connector.

Figure 10E of **Currie**:

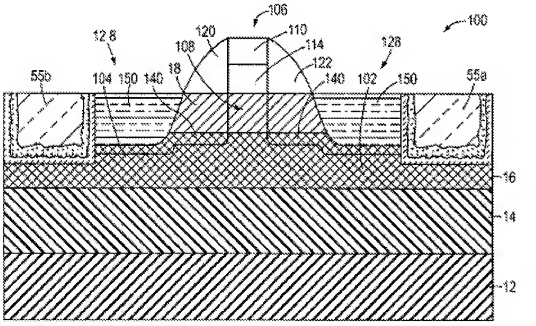

FIG. 10E

Paragraph 87 of **Currie**:

[0087] **Embodiments of this invention may also be applicable** to transistors with multiple or wrap-around gates. Examples of these include **fin-FETs**, tri-gate FETs, omega-FETs, and double-gate FETs (the channels of which may be oriented horizontally or vertically).

Figure 5 of **Chen**:

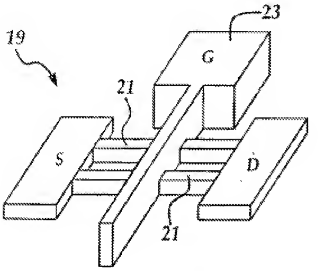

Figure 5

Appellants contend that Appellants are unable to find any reasonable support in either previously-cited Currie or Sugii or Chen, to form a localized stressor within the interior region of a fin connector of a FinFET, as required by the plain meaning of the claim language. Indeed, if anything, the references currently of record clearly demonstrate that there are many alternative ways to provide stressors in different types of devices. Rather, at most, primary reference Currie provides localized stressors in source/drain regions.

This is not found persuasive because Currie clearly teaches at fig. 10E, para. 77, forming at least one localized stressor region 150 within (inside trench/recess 144/148) said device (see fig. 10E), the at least one localized stressor region 150 being located

on one of fin connectors ((**at the end of fin 18,** note: 55a, 55b, 55c, 55d are isolation structures outside transistor), thus 150 is a part of fin connector, see para. 87:fin-FET, and see figure 5 of Chen: fin 21, fin connectors S(source)/D(drain), or figures. 27A-27C, 28 of Sugii: source/drain fin/fin connector 5/4/12)) as a region of stressor material 150 filling in an interior portion (trench/recess) of said fin connector (**at the end of fin 18**). Currie teaches at para. 87, embodiments of this invention may also be applicable to transistors with multiple or wrap-around gates. Examples of these include fin-FETs.

Thus, it would have been obvious to one having ordinary skill in the art at the time of invention was made to have recognized Currie's localized recess regions 144, 148 (within the device, fig. 10D) filled with strain/stress material 150 formed at the end of fin 18 (fig. 10B) of source/drain regions 102/104 would be obvious as a part of fin connector as taught by Chen et al. in figure 5 of Chen, or by Sugii et al. in figures 27A-27C and 28 of Sugii because source and drain regions are part of fin connector.

Appellants contend that Appellants respectfully traverse the Examiner's findings of facts, as follows:

1.

The Examiner points to regions 144,148 within primary reference Currie as allegedly demonstrating a localized stressor region of stressor material filling in an interior portion of a fin connector of a FinFET, further pointing to Figures 10D-10E and paragraphs [0016 and 0077] of Currie.

In response, Appellants respectfully submits that region 144, 148 is clearly defined in the second and third sentences of paragraph [0077] as recesses located in the source and drain regions 102,104, not a fin connector of a FinFET:

"For example, first and second recesses 144, 148 may be defined in source region 102 and drain region 104 that include Si .... Recesses 144, 148 may be filled with a second material 150 with a lattice constant larger than that of Si. such as SiGe, thereby inducing compressive strain in channel region 108."

This is not found persuasive because **Instant Invention** clearly teach in figure 5, paragraphs 20, 32, ion implanting entire FinFET with impurity dopant into the **unmasked** area to form **source/drain regions in fin 301 and fin connector 302** by using source/drain spacer 501 and gate 401 as an ion implantation mask.

Instant Invention discloses in paragraphs 20, 32 and figure 5 as follows:

[0020] **FIG. 5** exemplarily shows a plan view 500 in which the **source/drain spacers** have been formed;

[0032] The extensions (not shown in the figures) are implanted, using an ion implantation process. Preferably, As and/or P are used for nFinFETs and B and/or BF.sub.2 are used as ions for implants for pFinFETs. A plan view 500 of **FIG. 5** shows that the source/drain spacers 501 are next formed by depositing an oxide liner (e.g., silicon oxide) followed by depositing a SiN layer of about 500 .ANG.. Depending on the scaling, the range of the SiN layer might be anywhere in the 200 .ANG.600 .ANG.. A directional etch is then used to form the spacers 501. After spacer formation, **source-drain implants are performed using an ion implantation process** with dopants similar to that just described above. Raised source drains (not shown in the figures) are grown by selective epitaxial Si. Silicide (also not shown in the figures) is formed by reacting metal like, for example, Co, Ti, or Ni, or alloys or combinations thereof, with the exposed Si.

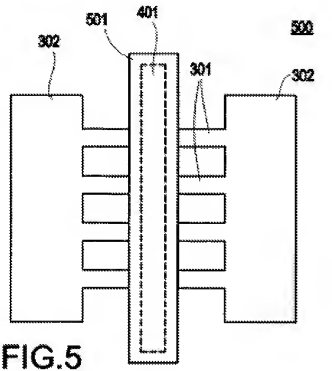

FIG.5

Currie clearly teaches in para. 16, 77, 87, figures 10D-10E, forming recess regions (within the device as claimed) 144, 148 at the end of fin 18 (note: 55a, 55b, 55c, 55d are isolation structures outside transistor), hence, regions 144, 148 are part of fin connector (see para. 87, finFET). Chen et al. shows in figure 5, S (source) and D (drain) of fin-FET are part of fin connectors connecting with fin 21.

Thus, it would have been obvious to one having ordinary skill in the art at the time of invention was made to have recognized Currie's localized recess regions 144, 148 (within the device, fig. 10D) formed at the end of fin 18 (figs. 10B-10E) of source/drain regions 102/104 would be obvious as a part of fin connector as taught by Chen et al. in figure 5 of Chen because source and drain regions are part of fin connector or by Suggi having source/drain fin/fin connector 5/4/12.

Therefore, there is not seen any difference between Currie's recess regions 144, 148 formed in the source/drain regions at the end of fin as a part of fin connector, and the etched (recess) region 601 formed in the source/drain region 302 of figures 5-6 of Instant invention.

Therefore, Currie clearly defined in the second and third sentences of paragraph [0077] as recesses 144 148 filled with stressor material 150 located in the source and drain regions 102,104 at the end of fin 18 would be a part of fin connector of a FinFET.

Appellants contends that Appellants respectfully expressly traverse the Examiner's finding of fact that Currie's paragraph [0077] teaches or suggests incorporating a localized stressor in a fin connector of a FinFET, let alone the interior portion of the fin connector.

This is not found persuasive because Currie clearly teaches in paragraphs 16, 77 and figure 10E, a localized stress (compressive or tensile strain/stress) 150 formed in the fin connector (**at the end of fin 18**, note: region 55a and 55b are isolation regions outside transistor). And, Chen et al. teaches at figure 5, source (S) and drain (D) regions are part of fin connector of FinFET device. Sugii et al. teaches at figures 27A-27C and 28, source and drain regions 5/4/12 are part of fin connector of FinFET device.

Thus, it would have been obvious to one having ordinary skill in the art at the time of invention was made to have recognized Currie's localized recess regions 144, 148 (within the device, fig. 10D) filled with stressor material 150 formed at the end of fin

18 (fig. 10B) of source/drain regions 102/104 would be obvious as a part of fin connector as taught by Chen et al. in figure 5 of Chen, or by Sugii et al. in figures 27A-27C and 28 of Sugii because source and drain regions are part of fin connector.

Currie teaches in paragraph 77:

[0077] With reference to FIGS. 10d-10e, in another embodiment, the strain in channel region 108 may be induced by the replacement of a portion of the semiconductor material in source region 102 and drain region 104, with a second material having a lattice constant different from that of the semiconductor material disposed in the channel region 108 or in an area 140 proximate at least one of the first source region 102 and first drain region 104. For example, first and second **recesses 144, 148 may be defined in source region 102 and drain region 104** that include Si (in which case channel region 108 also includes Si), as described in, e.g., U.S. Pat. Nos. 6,651,273 and 6,621,131, incorporated by reference herein. **Recesses 144, 148** may be **filled** with a **second material 150** with a lattice constant larger than that of Si, such as SiGe, thereby inducing **compressive strain** in channel region 108. Alternatively, **recesses 144, 148 in source region 102 and drain region 104** that include Si may be etched and refilled with second material 150 with a smaller lattice constant, such as silicon carbide (SiC), thereby inducing **tensile** strain in channel region 108. For source, drain, and channel regions that include SiGe, the refill second material 150 may be Ge or SiGe with a higher Ge content for inducing **compressive** strain or Si or SiGe with a lesser Ge content for inducing tensile strain. Area 140 may be, for example, a portion of relaxed layer 16 and/or a portion of strained layer 18. In an embodiment, first transistor 106 is formed on a bulk semiconductor substrate 12, and area 140 may include a portion of the bulk semiconductor substrate 12.

Currie teaches at figure 10E:

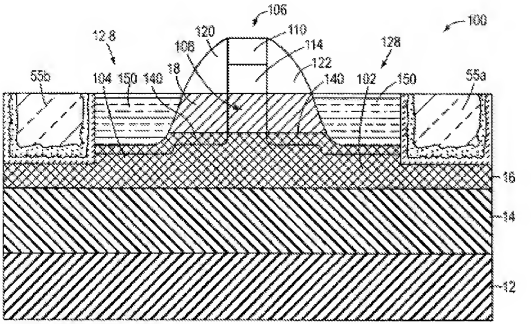

FIG. 10E

Chen discloses in figure 5, fin connector is source/drain regions:

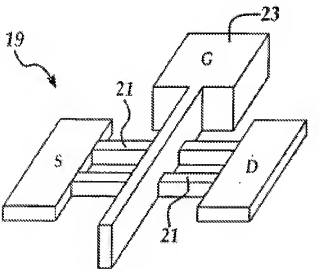

Figure 5

Appellants contend that Appellants are unable to find any suggestion in primary reference Currie to incorporate a localized stressor within the interior portion of a fin connector of a FinFET. Appellants respectfully request that the Board find that the rejection of record errs in its characterization that primary reference Currie demonstrates a localized stressor located on the interior portion of a fin connector of a FinFET. Moreover, Appellants also respectfully request that the rejection of record also, therefore, fails to properly identify the differences between primary reference Currie and the claimed invention, thereby failing to provide the proper foundation for an obviousness rejection.

This is not found persuasive because Examiner clearly explained and pointed in the **Final rejection and Advisory action** that Currie teaches at figure 10D-10E and para. 16, 77, 87, the localized stress 150 formed **at the end of fin 18** in the source/drain regions 144, 148 which would be a part of fin connector. And, Chen et al. teaches at figure 5, source (S) and drain (D) regions are part of fin connector of FinFET device. Sugii et al. teaches at figures 27A-27C and 28, source and drain regions 5/4/12 are part of fin connector of FinFET device.

Since Instant Invention teaches in figure 5 and paragraphs 20, 32, ion implanting the FinFET with impurity dopant into the **unmasked** area to form **source/drain regions in fin 301 and fin connector 302** by using source/drain spacer 501 and gate 401 as ion implantation masks.

And, **Currie** clearly teaches in para. 77, 87, figures 10D-10E, forming recess regions (within the device as claimed) 144, 148 filled with stressor material 150 at the end of fin 18 (note: 55a, 55b, 55c, 55d are isolation structures outside transistor), hence, regions 144, 148 would be part of fin connector (see para. 87, finFET) in view of Chen or Sugii.

Chen et al. shows in figure 5, fin connector (S, D) is source/drain region.

Sugii et al. shows in figures 27A-27C and 28, fin connector is source/drain region 5/4/12.

Therefore, there is not seen any difference between Currie's recess regions 144, 148 formed in the source/drain regions at the end of fin as a part of fin connector, and the etched (recess) region 601 formed in the source/drain region 302 of figures 5-6 of Instant invention.

Therefore, Currie clearly defined in the second and third sentences of paragraph [0077, 0087] as recesses 144 148 filled with stressor material 150 located in the source and drain regions 102,104 at the end of fin 18 would be a fin connector of a FinFET.

Thus, it would have been obvious to one having ordinary skill in the art at the time of invention was made to have recognized Currie's localized recess regions 144, 148 (within the device, fig. 10D) filled with stressor material 150 formed at the end of fin 18 (fig. 10B) of source/drain regions 102/104 would be obvious as a part of fin connector as taught by Chen et al. in figure 5 of Chen, or by Sugii et al. in figures 27A-27C and 28 of Sugii because source and drain regions are part of fin connector.

2.

Appellants contend that Appellants also respectfully request that the Board confirm that neither secondary reference Sugii nor secondary reference Chen teaches or suggests incorporating a localized stressor within the interior portion of a fin connector of a FinFET.

This is not found persuasive because Primary reference Currie et al. clearly teaches in paragraph 77, 87 and figs. 10E, forming at least one localized stressor region 144, 148 within (inside trench/recess) said device (see figs. 10D-10E, para. 16, 77), said at least one localized stressor region 150 being located on one of said fin connectors 144, 148 (at the end of fin 18, note: 55a, 55b, 55c, 55d are isolation structures outside transistor) as a region of stressor material 150 filling in an interior portion of said fin connector 144, 148 (at the end of fin 18, para. 77, 87 teach that embodiments of this invention may also be applicable to transistors with multiple or wrap-around gates. Examples of these include **fin-FETs**, tri-gate FETs, omega-FETs, and double-gate FETs (the channels of which may be oriented horizontally or vertically), hence, the localized stressor trench region 150 (SiGe, Si or SiC, see figure 10E, para. 16, 77) located on the fin connector (at the end of fin 18) would be applicable to the FinFET (Fin Field Effect Transistor). A plurality of fins 18 interconnected by fin connectors, such as fin-FETs, tri-gate FETs etc., Currie teaches: fin includes channel 108 and fin 18, fin connector/pad (source/drain) 150, gate 110, gate dielectric 114.

Chen et al. teaches in figs. 3-5, S (source) and D (drain) of fin-FET are part of fin connectors connecting with fins 21.

Sugii et al. teaches in figure 28, fin-FET having source/drain fin/fin connector 5/4/12.

Thus, it would have been obvious to one having ordinary skill in the art at the time of invention was made to have recognized Currie's localized recess regions 144, 148 (within the device, fig. 10D) filled with stressor material 150 formed at the end of fin 18 (fig. 10B) of source/drain regions 102/104 would be obvious as a part of fin connector as taught by Chen et al. in figure 5 of Chen et al., or by Sugii et al. in figures 27A-27C and 28 of Sugii because source and drain regions are part of fin connector.

3.

Appellants contend that Appellants also respectfully request that the Board confirm that the Examiner fails to provide in the rejection of record any motivation whatsoever to move the stressor in primary reference Currie from the source/drain regions of a device to the fin connector region.

This is not found persuasive because Examiner clearly provided the motivation to combine in pages 6-7 of the Final Rejection and is quoted below:

The difference between the reference(s) and the claims are as follows: Currie et al. teaches forming localized stressor trench regions on the fin connectors between transistors but does not show fin-FET having fin connectors in the drawing. However,

Sugii et al. teaches in figure 28, fin-FET having fin connectors. Sugii et al. also teaches at figs. 13-14, 19-29, para. 123-153, the source/drain regions 4 is a part of fin connector and forming localized stressor 5 on the of the fin connector 4. Sugii et al. also teaches forming a localized stressor 5 on the channel region, See figs. 13-14, 19-29. Chen et al. teaches at figs. 3-5 and para 26, a fin-FET having fin connectors and forming silicide layer on the fin connector.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have recognized that localized stressor trench (recess) region would be formed on a fin connector as shown in fig. 28 of Sugii et al. or figs. 3-5 of Chen et al. because fin connector connects source/drain regions of two FET transistors together.

And, Examiner also clearly provided in the Conclusion of Final Rejection and also in Advisory Action as follows:

Currie et al. teaches forming at least one localized stressor region 150 within (trench/recess) said device (see fig. 10E), the at least one localized stressor region 150 being located on one of fin connectors (at the end of fin 18, note: 55a, 55b, 55c, 55d are isolation structures outside transistor) connecting fin 18 as a region of stressor material filling in an interior portion of said fin connector (at the end of fin 18), para. 77. And para. 87 of Currie teach that embodiments of this invention may also be applicable to transistors with multiple or wrap-around gates. Examples of these include fin-FETs, tri-gate FETs, omega-FETs, and double-gate FETs (the channels of which may be oriented horizontally or vertically), hence, the localized stressor trench region 150 (see

fig. 10E) located on the fin connector (at the end of fin 18) that is between transistor 106 and transistor 106' that can be applicable to the FinFET (Fin Field Effect Transistor). A plurality of fins 18 interconnected by fin connectors, such as fin-FETs, tri-gate FETs etc. Currie et al. teaches, the fin includes channel 108 and fin 18, fin connector/pad (source/drain) 150, gate 110, gate dielectric 114. And Chen et al. teaches in figs. 3-5, fin-FET having fin connectors 36 or S or D connecting fin 12 or 21, Sugii et al. teaches in figure 28, fin-FET having fin connectors 4 connecting fin 5.

Since, Currie et al. teaches forming localized stressor regions (see fig. 10E, 11) within the device on the fin connector as comprising of stressor material filling in an interior portion of the fin connector can be applicable to transistors with multiple or wrap-around gates. Examples of these include fin-FETs, tri-gate FETs, omega-FETs, and double-gate FETs (the channels of which may be oriented horizontally or vertically), and Sugii et al. or Chen teaches a fin-FET having fin connectors, hence the combination of Currie and Sugii or Chen is proper. Therefore, it is clearly that the combination of Currie and Sugii or Chen meets the doctrine of U.S. Supreme Court in KSR international v. Teleflex of "a person of ordinary skill can implement a predictable variation, §103 likely bars its patentability". And, it is also clearly that the combination of Currie and Sugii or Chen meets the doctrine of U.S. Supreme Court in KSR international v. Teleflex of "If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious under §103".

Appellants contends that Indeed, if anything, primary reference Currie would teach placing the localized stressors adjacent to the channel region rather than the more distal location on fin connectors 601 such as shown in Figure 6 of the present application. That is, in Figure 8 of the present application, the source/drain regions are shown as regions 803,804 adjacent to the source/drain spacer 501 (see paragraph [0037]). According to the teachings of primary reference, the localized stressors would be placed in regions 803, 804 in a FinFET device, not in regions 302 as required by the independent claims.

This is not found persuasive because figure 8 of Instant Invention merely shows a small portion of source/drain regions 803, 840.

It was well known in the art that the semiconductor substrate has very little conductivity (that is why it is called semi-conductor). Thus, in order to use the semiconductor substrate as a fin connector to connect two transistors together, the fin connector formed in the semiconductor must be doped with impurity to have higher conductivity in the connector region. Hence, the fin connector 302 of Instant invention is a part of source/drain region that is doped with impurity (see explanation below).

In view of Instant Specification, Instant Invention clearly teaches in figure 5, paragraphs 20, 32, ion implanting entire FinFET with impurity dopant into the **unmasked** area to form **source/drain regions in fin 301 and fin connector 302** by using source/drain spacer 501 and gate 401 as ion implantation masks.

Instant Invention discloses in paragraphs 20, 32 and figure 5 as follows:

[0020] **FIG. 5** exemplarily shows a plan view 500 in which the **source/drain spacers** have been formed;

[0032] The extensions (not shown in the figures) are implanted, using an ion implantation process. Preferably, As and/or P are used for nFinFETs and B and/or BF.sub.2 are used as ions for implants for pFinFETs. A plan view 500 of **FIG. 5** shows that the source/drain spacers 501 are next formed by depositing an oxide liner (e.g., silicon oxide) followed by depositing a SiN layer of about 500 .ANG.. Depending on the scaling, the range of the SiN layer might be anywhere in the 200 .ANG.600 .ANG.. A directional etch is then used to form the spacers 501. After spacer formation, **source-drain implants are performed using an ion implantation process** with dopants similar to that just described above. Raised source drains (not shown in the figures) are grown by selective epitaxial Si. Silicide (also not shown in the figures) is formed by reacting metal like, for example, Co, Ti, or Ni, or alloys or combinations thereof, with the exposed Si.

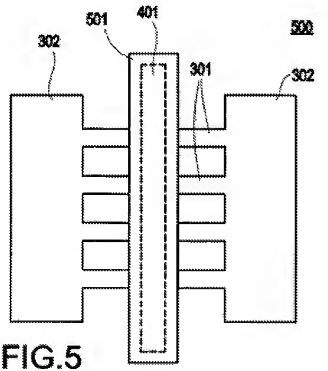

FIG.5

From above, it is clearly that **Figure 5** and paragraphs 20 and 32 of Instant Invention discloses **source/drain regions of Instant Invention includes fin 301 and fin connector 302.** Hence, **source/drain regions 803, 804 as shown in figure 8 of Instant Invention is only a small part of source/drain regions.**

Currie clearly teaches in para. 16, 77, 87, figures 10D-10E, forming recess regions (**within** the device as claimed) 144, 148 **at the end of fin** 18 (note: 55a, 55b, 55c, 55d are isolation structures outside transistor), hence, regions 144, 148 filled with stressor material 150 formed at the end of fin 18 are part of fin connector (see para. 87, finFET).

Chen et al. shows in figures 3- 5, fin connector is source/drain region that is located at the end fin 21 or 36.

Sugii et al. teaches in figures 27A-27C, 28, fin-FET having source/drain fin/fin connector 5/4/12.

Thus, it would have been obvious to one having ordinary skill in the art at the time of invention was made to have recognized Currie's localized recess regions 144, 148 (within the device, fig. 10D) filled with stressor material 150 formed at the end of fin 18 (fig. 10B) of source/drain regions 102/104 would be obvious as a part of fin connector as taught by Chen et al. in figure 5 of Chen, or by Sugii in figures 27A-27C and 28 of Sugii because source and drain regions are part of fin connector.

Therefore, there is not seen any difference between Currie's recess regions 144, 148 filled with stressor material 150 formed in the source/drain regions at the end of fin as a part of fin connector, and the etched (recess) region 601 formed in the source/drain region 302 of figures 5-6 of Instant invention.

Therefore, Currie clearly defined in the second and third sentences of paragraph [0016, 0077] as recesses 144 148 filled with stressor material 150 located in the source and drain regions 102,104 at the end of fin 18, is a part of fin connector of a FinFET.

4.

Appellants contends that that is, the Examiner fails to demonstrate any reference providing objective evidence that it was known in the art at the time of the present invention that primary reference Currie would be improved by relocating its localized stressor from the source/drain to a fin connector.

This is not found persuasive because Currie et al. clearly teaches forming at least one localized stressor region 150 within (trench/recess 144/148) said device (see fig. 10E), the at least one localized stressor region 150 being located on one of fin connectors (at the end of fin 18, note: 55a, 55b, 55c, 55d are isolation structures outside transistor) as a region of stressor material filling in an interior portion of said fin connector (at the end of fin 18), para. 77. And para. 87 of Currie teach that embodiments of this invention may also be applicable to transistors with multiple or wrap-around gates. Examples of these include **fin-FETs**, tri-gate FETs, omega-FETs, and double-gate FETs (the channels of which may be oriented horizontally or vertically), hence, the localized stressor trench region 150 (see fig. 10E) located on the fin connector (at the end of fin 18) that is applicable to the FinFET (Fin Field Effect Transistor). A plurality of fins 18 interconnected by fin connectors, such as fin-FETs, tri-gate FETs etc. Currie et al. teaches, the fin includes channel 108 and fin 18, fin connector/pad (source/drain) 150, gate 110, gate dielectric 114.

Chen et al. teaches in figs. 5, the fin connector is source/drain (S, D) region that is located at the end fin 21 or 36.

Sugii et al. teaches in figures 27A-27C, 28, fin-FET having source/drain fin/fin connector 5/4/12.

Thus, it would have been obvious to one having ordinary skill in the art at the time of invention was made to have recognized Currie's localized recess regions 144, 148 (within the device, fig. 10D) filled with stressor material 150 formed at the end of fin 18 (fig. 10B) of source/drain regions 102/104 would be obvious as a part of fin connector as taught by Chen et al. in figure 5 of Chen et al., or by Sugii et al. in figures 27A-27C and 28 of Sugii because source and drain regions are part of fin connector.

Therefore, Currie in view of Chen or Sugii clearly meets the claimed limitation of:

forming at least one localized stressor region 150 within (inside trench/recess 144/148) said device (see fig. 10E), the at least one localized stressor region 150 being **located on one of fin connectors** (at the end of fin 18) as a region of stressor material filling 150 in an interior portion (trench/recess 144, 148) of said fin connector (at the end of fin 18).

5.

Appellants contend that nor does the Examiner provide any reference providing objective evidence that it was known in the art at the time of the present invention that incorporating a localized stressor on the interior portion of a fin connector of a FinFET was known as a substitute for a localized stressor on a source/drain of a simple FET.

This is not found persuasive because Currie in view of Chen or Sugii clearly meets the claimed limitation of " forming at least one localized stressor region 150 **within** (inside **trench/recess** 144/148) said device (see fig. 10E), the at least one localized stressor region 150 being **located on one of fin connectors** (at the end of fin 18, note: 55a, 55b, 55c, 55d are isolation structures outside transistor) connecting fin 18 as a region of stressor material 150 filling in an interior portion (trench/recess 144, 148) of said fin connector (at the end of fin 18).

Currie clearly teaches in para. 77, 87, figures 10D-10E, forming recess regions (**within** the device as claimed) 144, 148 filled with stressor material 150 **at the end of fin** 18, hence, regions 144, 148 are part of fin connector (see para. 87, finFET) in view of Chen or Sugii.

Chen et al. shows in figures 3- 5, source/drain regions (S, D) is fin connectors that is located at the end fin 21 or 36.

Sugii et al. teaches in figures 27A-27C, 28, fin-FET having source/drain fin/fin connector 5/4/12.

Thus, it would have been obvious to one having ordinary skill in the art at the time of invention was made to have recognized Currie's localized recess regions 144, 148 (within the device, figs. 10D-10E) filled with stressor material 150 formed at the end of fin 18 (fig. 10B, note: 55c, 55d are isolation structures outside transistor) of source/drain regions 102/104 would be obvious as a part of fin connector as taught by Chen et al. in figure 5 of Chen, or by Sugii in figures 27A-27C and 28 of Sugii because source and drain regions are part of fin connector.

Therefore, there is not seen any difference between Currie's recess regions 144, 148 filled with stressor material 150 formed in the source/drain regions at the end of fin as a part of fin connector, and the etched (recess) region 601 formed in the source/drain region 302 of figures 5-6 of Instant invention.

Therefore, Currie clearly defined in the second and third sentences of paragraph [0016, 0077] as recesses 144 148 filled with stressor material 150 located in the source and drain regions 102,104 at the end of fin 18, is a part of fin connector of a FinFET.

Appellants contend that the most that can reasonably be deduced from the references of record is that FinFETs were known in the art at the time of the invention and that the claimed invention, therefore, would have been possible. Indeed, on page 7 of the latest Office Action, the Examiner clearly states that the standard being applied in the present evaluation is based on the conclusion that one of skill "would have recognized" that the claimed invention was possible: "It would have been obvious to one having ordinary skill in the art at the time of the invention was made to have recognized that localized stressor trench (recess) region can be formed on a fin connector as shown in fig. 28 of Sugii et al. or figs. 3-5 of Chen et al. because [a] fin connector connects source/drain regions of two FET transistors together." However, such demonstration of mere possibility at the time of the invention is insufficient, since the correct standard for obviousness requires an articulation of a reasonable rationale to modify the primary reference to arrive at the claimed invention, and the rejection of record is based on the wrong standard for obviousness. A mere conclusory statement

that one of skill would have "recognized that the claimed invention was possible at the time of the invention" is nothing but a rationale based on improper hindsight. In the final two paragraphs of the Advisory Action mailed on February 23, 2010, the Examiner states:

"Since, [sic] Currie et al. teaches forming localized stressor regions (see.fig. I OE, 11) within the device on the fin connector as comprising of stressor material filling in an interior portion of the fin connector can be applicable to transistors with multiple or wrap-around gates [sic]. Examples of these include fin-FETs, tri-gate FETs, omega-FETs, and double-gate FETs (the channel of which may be oriented horizontally or vertically), and Sugii et al., or Chen teaches a fin-FET having fin connectors, hence the combination of Currie and Sugii or Chen is proper. Therefore, it is clearly[sic] that the combination of Cuttle and Sugii or Chen meets the doctrine of U.S. Supreme Court in KSR international [sic] v Teleflex of "a person of ordinary skill can implement a predictable variation, §103 likely bars its patentability". And, it is also clearly [sic] that the combination of Currie and Sugii or Chen meets the doctrine of U.S. Supreme Court in KSR international [sicJv. Teleflex of "if this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious under §103.'"

In response, Appellants first again respectfully traverse the Examiner's characterization in the first sentence recited above from the Advisory Action that primary reference Currie teaches incorporation of a localized stressor on an interior portion of a fin connector of a FinFET, since Currie's Figures 10-11 are both demonstrating source/drains of a simple FET, not fin connectors of a FinFET, as would be required to satisfy independent claim 1.

This is not found persuasive because Currie in view of Chen or Sugii clearly meets the claimed limitation of " forming at least one localized stressor region 150 **within** (inside **trench/recess** 144/148) said device (see fig. 10E), the at least one localized stressor region 150 being **located on one of fin connectors** (at the end of fin 18, note: 55a, 55b, 55c, 55d are isolation structures outside transistor) as a region of stressor material 150 filling in an interior portion (trench/recess 144, 148) of said fin connector (at the end of fin 18).

Currie clearly teaches in para. 16, 77, 87, figures 10D-10E, forming recess regions (**within** the device as claimed) 144, 148 filled with stressor material 150 **at the end of fin** 18, hence, regions 144, 148 are part of fin connector (see para. 87, finFET) in view of Chen or Sugii.

Chen et al. shows in figures 3- 5, source/drain regions (S, D) is fin connector that is located at the end fin 21 or 36.

Sugii et al. teaches in figures 27A-27C, 28, fin-FET having source/drain fin/fin connector 5/4/12.

Thus, it would have been obvious to one having ordinary skill in the art at the time of invention was made to have recognized Currie's localized recess regions 144, 148 (within the device, fig. 10D-10E) filled with stressor material 150 formed at the end of fin 18 (fig. 10B, note: 55c, 55d are isolation structures outside transistor) of source/drain regions 102/104 would be obvious as a part of fin connector as taught by Chen et al. in figure 5 of Chen, or by Sugii in figures 27A-27C and 28 of Sugii because source and drain regions are part of fin connector.

Therefore, there is not seen any difference between Currie's recess regions 144, 148 formed in the source/drain regions at the end of fin as a part of fin connector, and the etched (recess) region 601 formed in the source/drain region 302 of figures 5-6 of Instant invention.

Therefore, Currie clearly defined in the second and third sentences of paragraph [0077] as recesses 144 148 filled with stressor material 150 located in the source and drain regions 102,104 at the end of fin 18 would be a part of fin connector of a FinFET.

Appellants contend that Second, Appellants respectfully submit that the combination of Currie and Sugii or Chen, even if considered proper, would only result in placing the localized stressor region of Currie on the source/drain regions of all of the devices demonstrated in the cited references. As explained above, relative to the FinFET shown in Figure 8 of the present application, this means that the localized stressors of Currie would be placed in regions 803, 804, not in the interior of fin connectors 302. In contrast, the Examiner's initial burden in the obviousness rejection of the present evaluation is to provide a reasonable rationale to relocate the localized stressors of Currie to be on the interior portion of a fin connector of a FinFET, thereby resulting in the claimed invention. Merely demonstrating existence of FinFETs is insufficient to meet this burden. None of the references of record suggest that it was a known improvement or substitution to make the necessary modification to arrive at the invention described in claim 1. In the configuration shown in Figure 8 of the present application, the Examiner's initial burden would be to provide a reasonable rationale to

relocate localized stressors placed in source/drain regions 803,804 (in accordance with the source/drain localized stressors of primary reference Currie) to be in fin connectors 302.

This is not found persuasive because figure 8 of Instant Invention merely shows a small portion of source/drain regions 803, 840.

It is well known in the art that the semiconductor substrate has very little conductivity (that why is called semi-conductor). Thus, in order to use the semiconductor substrate as a fin connector to connect two transistors together, the fin connector formed in the substrate must be doped with impurity to have higher conductivity in the fin connector region. Hence, the fin connector 302 of Instant invention is a part of source/drain region that is doped with impurity (see explanation below).

In view of Instant Specification, Instant Invention clearly teaches in figure 5, paragraphs 20, 32, ion implanting entire FinFET with impurity dopant into the **unmasked** area to form **source/drain regions in fin 301 and fin connector 302** by using source/drain spacer 501 and gate 401 as ion implantation masks.

Instant Invention discloses in paragraphs 20, 32 and figure 5 as follows:

> [0020] **FIG. 5** exemplarily shows a plan view 500 in which the **source/drain spacers** have been formed;
>
> [0032] The extensions (not shown in the figures) are implanted, using an ion implantation process. Preferably, As and/or P are used for nFinFETs and B and/or BF.sub.2 are used as ions for implants for pFinFETs. A plan view 500 of **FIG. 5** shows that the source/drain spacers 501 are next formed by depositing an oxide liner (e.g., silicon oxide) followed by depositing a SiN layer of about 500 .ANG.. Depending on the scaling, the range of the SiN layer might be

anywhere in the 200 .ANG.600 .ANG.. A directional etch is then used to form the spacers 501. After spacer formation, **source-drain implants are performed using an ion implantation process** with dopants similar to that just described above. Raised source drains (not shown in the figures) are grown by selective epitaxial Si. Silicide (also not shown in the figures) is formed by reacting metal like, for example, Co, Ti, or Ni, or alloys or combinations thereof, with the exposed Si.

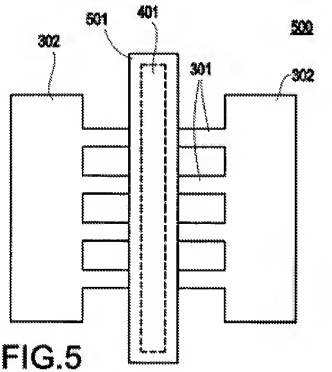

FIG.5

From above, it is clearly that Figure 5 and paragraphs 20 and 32 of Instant Invention discloses **source/drain regions of Instant Invention includes fin 301 and fin connector 302.** Hence, **source/drain regions 803, 804 as shown in figure 8 of Instant Invention is only a small part of source/drain regions.**

Currie clearly teaches in para. 16, 77, 87, figures 10D-10E, forming recess regions (**within** the device as claimed) 144, 148 filled with stressor material 150 **at the end of fin** 18 (note: 55a, 55b, 55c, 55d are isolation structures outside transistor),

hence, regions 144, 148 formed at the end of fin 18 are part of fin connector (see para. 87, finFET) in view of Chen or Sugii.

Chen et al. shows in figures 3- 5, source/drain regions (S,D) is fin connector that is located at the end fin 21 or 36.

Sugii et al. teaches in figures 27A-27C, 28, fin-FET having fin connectors 5/4/12.

Thus, it would have been obvious to one having ordinary skill in the art at the time of invention was made to have recognized Currie's localized recess regions 144, 148 (within the device, figs. 10D-10E) filled with stressor material 150 formed at the end of fin 18 (fig. 10B-10E) of source/drain regions 102/104 would be obvious as a part of fin connector as taught by Chen et al. in figure 5 of Chen, or by Sugii in figures 27A-27C and 28 of Sugii because source and drain regions are part of fin connector.

Therefore, there is not seen any difference between Currie's recess regions 144, 148 formed in the source/drain regions at the end of fin as a part of fin connector, and the etched (recess) region 601 formed in the source/drain region 302 of figures 5-6 of Instant invention.

Therefore, Currie clearly defined in the second and third sentences of paragraph [0077] as recesses 144 148 filled with stressor material 150 located in the source and drain regions 102,104 at the end of fin 18, would be a part of fin connector of a FinFET.

Appellants contend that relative to the Examiner's reliance upon the KSR holding, as recited above, Appellants respectfully submit that the references of record do not demonstrate that relocating a localized stressor from a source or drain was known in the

art at the time of the present invention to be a "predictable variation" or that it would be "obvious to try" the relocation necessary to arrive at the claimed invention. Without providing some objective evidence that the relocation of stressors from a source/drain to an interior portion of a fin connector, the Examiner's statements above are merely conclusory statements based on improper hindsight.

This is not found persuasive because Currie clearly teaches in para. 16, 77, 87, figures 10D-10E, forming recess regions (**within** the device as claimed) 144, 148 filled with stressor material 150 **at the end of fin** 18 (note: 55a, 55b, 55c, 55d are isolation structures outside transistor), hence, regions 144, 148 formed at the end of fin 18 would be a part of fin connector (see para. 87, finFET) in view of Chen or Sugii.

Chen et al. shows in figures 3- 5, source/drain regions (S, D) is a part of fin connector that is located at the end fin 21 or 36.

Sugii et al. teaches in figures 27A-27C, 28, fin-FET having source/drain fin/fin connector 5/4/12.

Thus, it would have been obvious to one having ordinary skill in the art at the time of invention was made to have recognized Currie's localized recess regions 144, 148 (within the device, figs. 10D-10E) filled with stressor material 150 formed at the end of fin 18 (fig. 10B) of source/drain regions 102/104 would be obvious as a part of fin connector as taught by Chen et al. in figure 5 of Chen, or by Sugii in figures 27A-27C and 28 of Sugii because source and drain regions are part of fin connector.

Therefore, there is not seen any difference between Currie's recess regions 144, 148 formed in the source/drain regions at the end of fin as a part of fin connector, and the etched (recess) region 601 formed in the source/drain region 302 of figures 5-6 of Instant invention.

Therefore, Currie clearly defined in the second and third sentences of paragraph [0077] as recesses 144 148 filled with stressor material 150 located in the source and drain regions 102,104 at the end of fin 18, would be a part of fin connector of a FinFET.

Therefore, Currie in view of Chen or Sugii clearly demonstrate that a localized stressor 150 formed in source or drain regions 102/104/144/148 at the end of fin is a part of fin connector that is known in the art at the time of the present invention to be a "predictable variation" or that it would be "obvious to try" the relocation necessary to arrive at the claimed invention as required in KSR v. Teleflex.

Appellants contend that Indeed, the holding in KSR also states (emphasis by Appellants): "When it first established the requirement of demonstrating a teaching, suggestion, or motivation to combine known elements in order to show that the combination is obvious, the Court of Customs and Patent Appeals captured a helpful insight. See Application of Bergel, 292 F. 2d 955, 956-957 (1961). As is clear from cases such as Adams, a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently known in the prior art. Although common sense directs one to look with care at a patent application that claims as innovation the combination of two known devices according to their

established functions, it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the wav the claimed new invention does. This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known."

This is not found persuasive because KSR international v. Teleflex, US Supreme Court, April 30, 2007 states, the TSM test (teaching, suggest or motivation) captures a helpful insight: A patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art. Although common sense directs caution as to a patent application claiming as innovation the combination of two known devices according to their established functions, it can be important to identify a reason that would have prompted a person of ordinary skill in the art to combine the elements as the new invention does. Inventions usually rely upon building blocks long since uncovered, and claimed discoveries almost necessarily will be combinations of what, in some sense, is already known. Helpful insights, however, need not become rigid and mandatory formulas. If it is so applied, the TSM test is incompatible with this Courts precedents. The diversity of inventive pursuits and of modern technology counsels against confining the obviousness analysis by a formalistic conception of the words teaching, suggestion, and motivation, or by overemphasizing the importance of published articles and the explicit content of issued patents. In many fields there may be little discussion of obvious techniques or combinations, and market demand, rather than scientific literature, may often drive design trends.

The Court of Appeals, finally, drew the wrong conclusion from the risk of courts and patent examiners falling prey to hindsight bias. A factfinder should be aware, of course, of the distortion caused by hindsight bias and must be cautious of arguments reliant upon *ex post* reasoning. See *Graham*, 383 U. S., at 36 (warning against a temptation to read into the prior art the teachings of the invention in issue. and instructing courts to . .guard against slipping into the use of hindsight. . (quoting *Monroe Auto Equipment Co.* v. *Heckethorn Mfg. & Supply Co.*, 332 F. 2d 406,412 (CA6 1964))). Rigid preventative rules that deny factfinders recourse to common sense, however, are neither necessary under our case law nor consistent with it. We note the Court of Appeals has since elaborated a broader conception of the TSM test than was applied in the instant matter. See, *e.g., DyStar Textilfarben GmbH & Co. Deutschland KG* v. *C. H. Patrick Co.*, 464 F. 3d 1356, 1367 (2006) (.Our suggestion test is in actuality quite flexible and not only permits, but *requires*, consideration of common knowledge and common sense.); *Alza Corp.* v. *Mylan Labs., Inc.*, 464 F. 3d 1286, 1291 (2006)(.There is flexibility in our obviousness jurisprudence because a motivation may be found *implicitly* in the prior art. We do not have a rigid test that requires an actual teaching to combine . . ..). Those decisions, of course, are not now before us and do not correct the errors of law made by the Court of Appeals in this case. The extent to which they may describe an analysis more consistent with our earlier precedents and our decision here is a matter for the Court of Appeals to consider in its future cases. What we hold is that the fundamental misunderstandings identified above led the Court of Appeals in this case to apply a test inconsistent with our patent law decisions.

Appellants contend that Appellants have demonstrated that none of the references relied upon in the rejection of record demonstrates the element of the claimed invention of a localized stressor as an interior portion of a fin connector of a FinFET. Nor does the rejection of record even properly identify the differences between primary reference Currie and the claimed invention. Finally, Appeliants submit that the rejection of record fails to provide a reasonable rationale to modify primary reference Currie to arrive at the invention defined in independent claim 1.

This is not found persuasive because in the Final Rejection mailed on Dec. 14, 2009, Examiner clearly and properly identify the primary reference Currie in view of Chen or Sugii teaches all the limitations as claimed in claimed invention, and demonstrated that Currie teaches a localized stress 150 locating in the recess 144, 148 at the end of fin 18 of source/drain regions 102/104 meeting the element of the claimed invention of a localized stressor as an interior portion of a fin connector of a FinFET.

Currie et al. clearly teaches forming at least one localized stressor region 150 within (inside trench/recess) said device (see fig. 10E), the at least one localized stressor region 150 being located on one of fin connectors (at the end of fin 18, note: 55a, 55b, 55c, 55d are isolation structures outside transistor) as a region of stressor material 150 filling in an interior portion (recess 144, 148) of said fin connector (at the end of fin 18), para. 16, 77. And para. 87 of Currie teach that embodiments of this invention may also be applicable to transistors with multiple or wrap-around gates. Examples of these include **fin-FETs**, tri-gate FETs, omega-FETs, and double-gate

FETs (the channels of which may be oriented horizontally or vertically), hence, the localized stressor trench region 150 (see fig. 10E) located in the fin connector (at the end of fin 18) is applicable to the FinFET (Fin Field Effect Transistor). A plurality of fins 18 interconnected by fin connectors, such as fin-FETs, tri-gate FETs etc. Currie et al. teaches the fin includes channel 108 and fin 18, fin connector/pad (source/drain) 150, gate 110, gate dielectric 114.

Chen et al. teaches in figs. 3-5, source/drain regions (S, D) are fin connectors of fin-FET for connecting fins 12 or 21.

Sugii et al. teaches in figures 27A-27C, 28, fin-FET having source/drain fin/fin connector 5/4/12.

Thus, it would have been obvious to one having ordinary skill in the art at the time of invention was made to have recognized Currie's localized recess regions 144, 148 (within the device, figs. 10D-10E) filled with stressor material 150 formed at the end of fin 18 (fig. 10B-10E) of source/drain regions 102/104 would be obvious as a part of fin connector as taught by Chen et al. in figure 5 of Chen et al., or by Sugii et al. in figures 27A-27C and 28 of Sugii because source and drain regions are part of fin connector.

Therefore, Currie in view of Chen or Sugii clearly meets the claimed limitation of claimed 1:

forming at least one localized stressor region 150 within (trench/recess) said device (see fig. 10E), the at least one localized stressor region 150 being **located on one of fin connectors** (at the end of fin 18) as a region of stressor material 150 filling in an interior portion (trench/recess 144, 148) of said fin connector (at the end of fin 18).

ISSUE #2:

THE REJECTION FOR INDEPENDENT CLAIM 14 AND DEPENDENT CLAIM 6, AS BASED ON CURRIE, FURTHER IN VIEW OF EITHER SUGII OR CHEN.

Appellants contend that Appellants respectfully submit that the errors discussed above for ISSUE #1 apply equally to ISSUE #2. Additionally, this issue includes the failure of the rejection of record to provide motivation to relocate one of the two localized stressors of primary reference Currie from the source to be on one fin connector of a FinFET and to relocate the localized stressor from the drain to a second fin connector of the FinFET.

This is not found persuasive because Appellants have failed to provide any reasoning, comparison and rebuttal between the cited references and Instant Invention.

In Final Rejection mailed on Dec. 14, 2009, Examiner clearly and properly identify primary reference Currie in view of Chen or Sugii teaches all the limitation as claimed in the claimed invention, and demonstrated that Currie teaches localized stressors 150 locating in the recess 144, 148 at the end of fin 18 meeting the element of the claimed invention of a localized stressor as an interior portion of a fin connector of a FinFET.

Currie et al. clearly teaches at figs. 10B-10E and para. 16, 77, forming localized stressor regions 150 within (inside trench/recess 144/148) the source region (102/144, first localized stressor) and drain region (104/148, second localized stressor) of the

device (see fig. 10E), the first and second localized stressor regions 150 being located at both ends of fin 18 (note: 55a, 55b, 55c, 55d are isolation structures outside transistor) as regions of stressor material 150 filling in interior portion (recess 144, 148) of said fin connectors (at the end of fin 18). And para. 87 of Currie teach that embodiments of this invention may also be applicable to transistors with multiple or wrap-around gates. Examples of these include **fin-FETs**, tri-gate FETs, omega-FETs, and double-gate FETs (the channels of which may be oriented horizontally or vertically), hence, the localized stressor trench region 150 (see fig. 10E) located on the fin connector (at the both end of fin 18) is applicable to the FinFET (Fin Field Effect Transistor). A plurality of fins 18 interconnected by fin connectors, such as fin-FETs, tri-gate FETs etc. Currie et al. teaches the fin includes channel 108 and fin 18, fin connector/pad (source/drain) 150, gate 110, gate dielectric 114.

Chen et al. teaches in figs. 3-5, source/drain regions (S, D) as part of fin connectors for connecting fin 12 or 21.

Sugii et al. teaches in figures 27A-27C, 28, fin-FET having source/drain fin/fin connector 5/4/12.

Thus, it would have been obvious to one having ordinary skill in the art at the time of invention was made to have recognized Currie's localized recess regions 144, 148 (within the device, figs. 10D-10E) filled with stressor material 150 formed at the both end of fin 18 (fig. 10B) of source/drain regions 102/104 would be obvious as parts of fin connector as taught by Chen et al. in figure 5 of Chen et al., or by Sugii et al. in figures 27A-27C and 28 of Sugii because source/drain regions are part of fin connector.

Therefore, Currie in view of Chen or Sugii clearly meets the claimed limitation of claims 14 and 6:

forming a first localized stressor region 144/150 (at the end of fin 18, see figs. 10D-10E, para. 16, 77, 87) within (inside trench/recess 144) said device on a first fin connector (at the end of fin 18) as comprising a first region of stressor material 150 filling in an interior portion (trench/recess 144) of said first fin connector (at the end of fin 18); and forming a second localized stressor region 148/150 within (trench recess 148) said device on a second fin connector (at the end of fin 18) as comprising a second region of stressor material 150 filling in an interior portion (trench/recess 148) of said second fin connector, said first localized stressor region and said second localized stressor region causing a region 108 there between to be stressed.

ISSUE #3:

THE REJECTION FOR DEPENDENT CLAIM 30, AS BASED ON CURRIE, FURTHER IN VIEW OF EITHER SUGII OR CHEN.

Appellants contend that Appellants expressly traverse the Examiner's finding of fact that paragraph [0077] of primary reference Currie reasonably makes any suggestion of asymmetric stressing using localized stressors.

This is not found persuasive because Appellants have failed to provide any reasoning, comparison and rebuttal between the cited references and Instant Invention for the asymmetric stressing using localized stressors.

Currie teaches in paragraphs 14-16, 22-23 of summary of Invention and paragraph 77, forming a first trench **at least one** of first source region and first drain region and the strain in the first channel region my be induced by **at least on**e of first source region and first drain region, hence, when **only one** of source and drain trench regions is filled with strain/stress material, the channel region would see asymmetric stressing from **only one** of localized stressor in the source trench or drain trench.

[0014] In an aspect, the invention features a structure including a substrate, and a first transistor disposed over a first region of the substrate. The first transistor includes a first source region and a first drain region disposed in a first portion of the substrate, a first channel region disposed between the first source region and the first drain region, the first channel region having a first type of strain, and a first gate disposed above the first channel region and between the first source and first drain regions, the first gate including a material selected from the group of a doped semiconductor, a metal, and a metallic compound. A first trench structure is proximate **at least one side** of one of the first **source region** and the first **drain region**. The first trench structure **induces only a portion** of the first type of **strain** in the first channel region.

[0016] A first cap layer may be disposed over a surface of the first transistor, and the strain in the first channel region may be induced by the first cap layer. The first cap layer may include silicon nitride. The strain in the first channel region may be induced by at least one of the first source region and the first drain region. The at least one of the first source region and the first drain region may include a second material having a larger lattice constant than a lattice constant of a semiconductor material disposed in at least one of the first channel region and an area proximate at least one of the first source region and the first drain region. The second material may include a material selected from the group including SiGe and Ge. The **at least one of** the first **source region** and the first **drain region** may include a second material having a smaller lattice constant than a lattice constant of a semiconductor material disposed in **at least one of** the first channel region and an area proximate at least one of the first source region and the first drain region. The second material may include a material selected from the group of SiGe, Si, and SiC.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/H. Jey Tsai/

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RQAS, TC 2800